

TFT LCD Tentative Specification

MODEL NO.: N141XC -L01

Customer : _____

Approved by : _____

Note :

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
	



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OPTOELECTRONICS CORP

Issued Date: May. 27, 2005

Model No.: N141XC -L01

Tentative**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
Ver 0.0	May. 27. '05	All	All	Tentative specification first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

N141XC -L01 is a 14.1" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1024 x 768 XGA mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and light weight
- XGA (1024 x 768 pixels) resolution
- DE (Data Enable) only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 1 pixel/clock
- Support EDID Structure Version 1 Revision 3

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

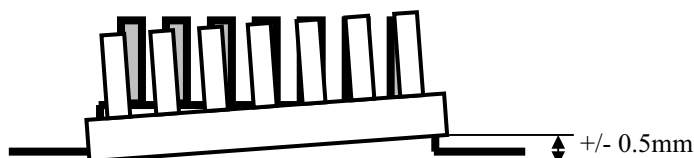
Item	Specification	Unit	Note
Outline Dimension	299(W) x 228 (H)	mm	(1)
Active Area	285.7 (H) x 214.3 (V) (14.1" diagonal)	mm	
Bezel Opening Area	288.9 (H) x 217.5 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1024 x R.G.B. x 768	pixel	-
Pixel Pitch	0.279 (H) x 0.279 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hardness (2H), Anti-glare (Haze 40), Reflection < 3%	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	298.5	299.0	299.5	mm	(1)
	Vertical(V)	227.5	228.0	228.5	mm	
	Depth(D)	4.9	5.2	5.5	mm	
Weight		385	400	415	g	-
I/F connector mounting position		The mounting inclination of the connector makes the screen center within ±0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

(2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

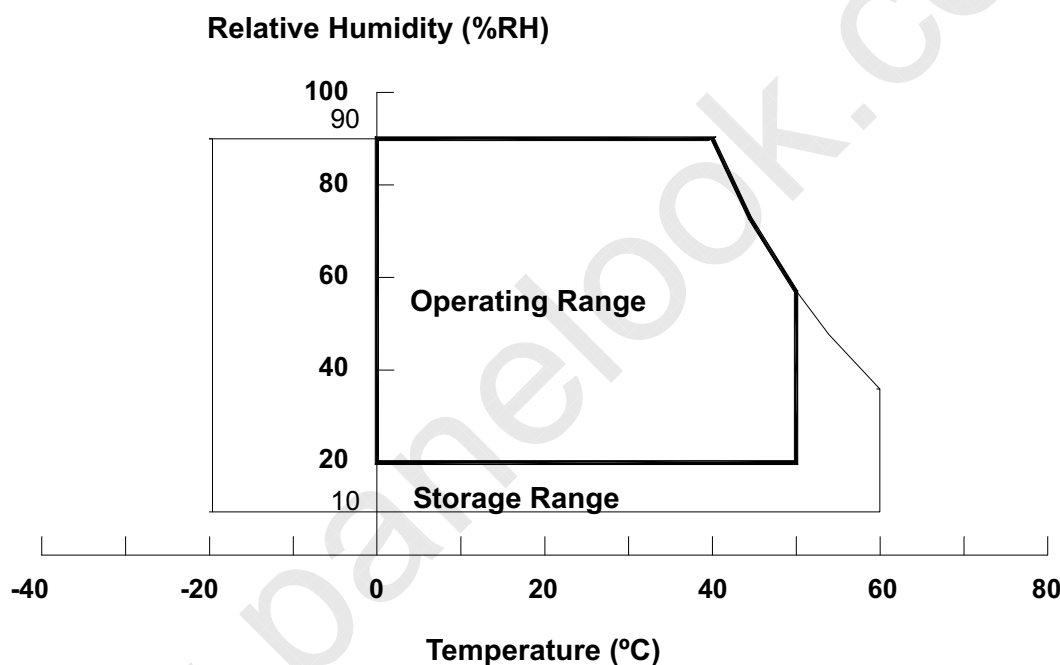
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	220	G	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation .

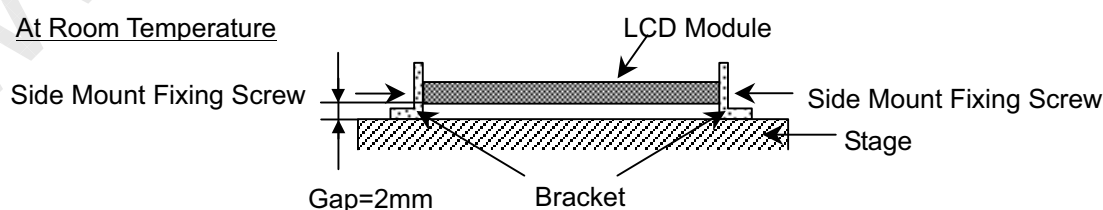


Note (2) The temperature of panel surface should be 0 °C Min. and 50 °C Max.

Note (3) 2ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 500 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z. The fixing condition is shown as below:

At Room Temperature



Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V _{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CC} +0.3	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V _L	-	2.5K	V _{RMS}	(1), (2), I _L = (6.0) mA
Lamp Current	I _L	-	6.5	mA _{RMS}	
Lamp Frequency	F _L	-	80	KHz	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to Section 3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

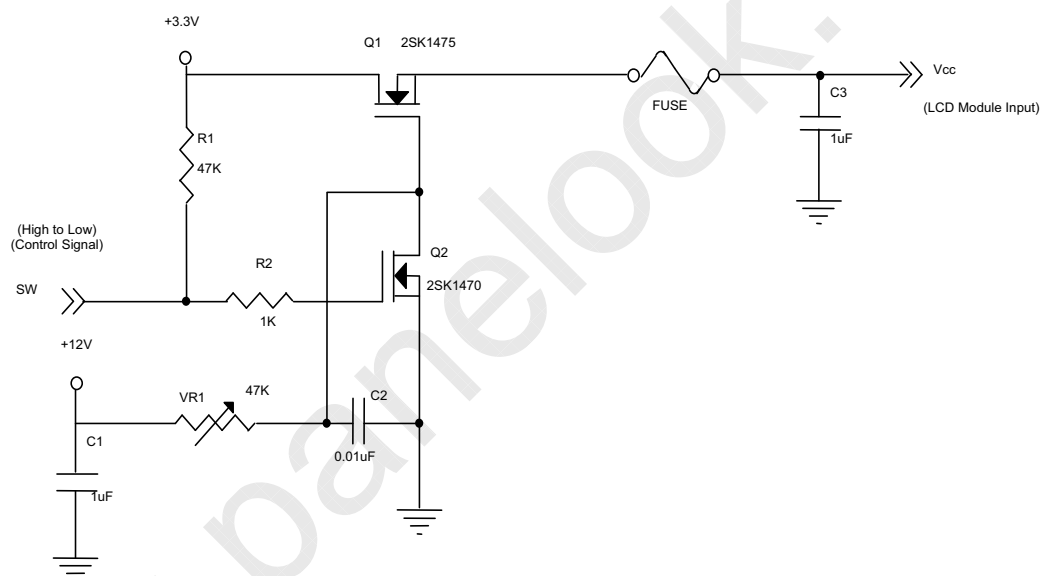
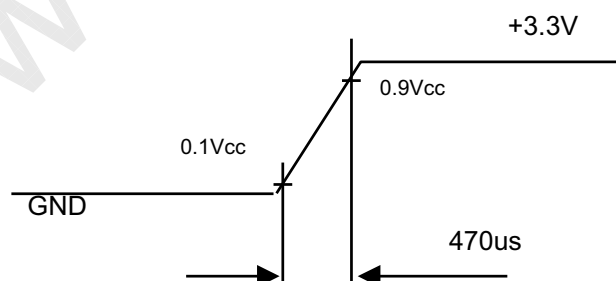
3.1 TFT LCD MODULE

Ta = 25 ± 2 °C

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	3.0	3.3	3.6	V	-
Ripple Voltage		V _{RP}	-	-	100	mV	-
Rush Current		I _{RUSH}	-	-	1.5	A	(2)
Power Supply Current	White	I _{CC}	-	(270)		mA	(3)a
	Black		-	(330)		mA	(3)b
	Vertical Stripe		-	(350)		mA	(3)c
Differential Input Voltage for LVDS Receiver Threshold	"H" Level	V _{IH}	-	-	+100	mV	-
	"L" Level	V _{IL}	-100	-	-	mV	-
Terminating Resistor		R _T	-	100	-	Ohm	-
Power per EBL WG		P _{EBL}	-	TBD	-	W	(4)

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:

**Vcc rising time is 470us**

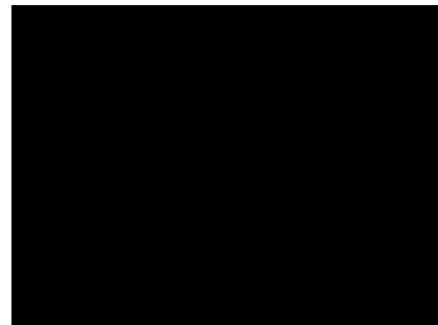
Note (3) The specified power supply current is under the conditions at $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, DC Current and $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



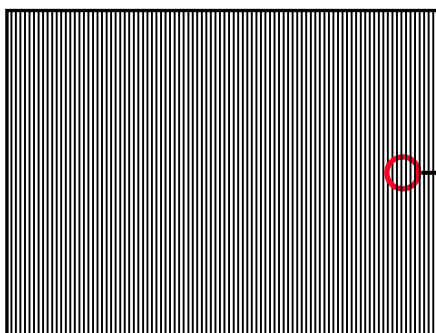
Active Area

b. Black Pattern

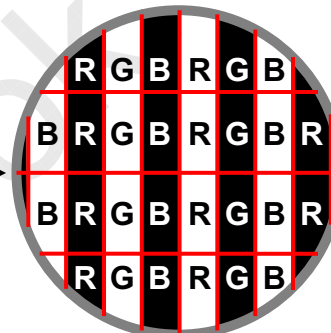


Active Area

c. Vertical Stripe Pattern



Active Area



Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.

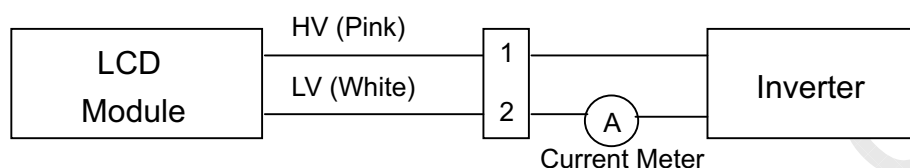
- (a) $V_{cc} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from O2Micro(www.o2micro.com). CMO doesn't provide the inverter in this product.

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V _L	(576)	(640)	(704)	V _{RMS}	I _L = 6.0 mA
Lamp Current	I _L	2.0	(6.0)	(6.5)	mA _{RMS}	(1), (8)
Lamp Turn On Voltage	V _S	-	-	(1360(25 °C))	V _{RMS}	(2)
		-	-	(1450 (0 °C))	V _{RMS}	(2)
Operating Frequency	F _L	(50)	-	80	KHz	(3)
Power Consumption	P _L	-	(3.84)	-	W	(4), I _L = 6.0 mA
Lamp Life Time	L _{BL}	(12,000)	-	-	Hrs	(5)
Leakage Current	I _{IN} -I _{OUT}	-	(1.0)	(1.25)	mA	(7)

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) The voltage shown above should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may generate interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L$

Note (5) The lifetime of lamp is defined as the time when it continues to operate under the conditions at Ta = 25 ± 2 °C and I_L = 6.0 mA_{RMS} until one of the following events occurs:

- (a) When the brightness becomes ≤ 50% of its original value.
- (b) When the effective ignition length becomes ≤ 80% of its original value. (Effective ignition length is defined as an area that the brightness is less than 70% compared to the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below;
- b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;



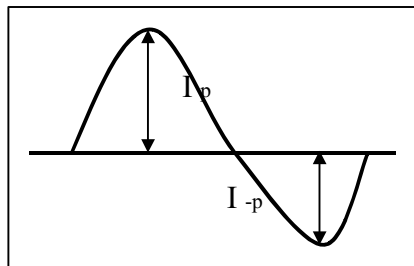
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c. The ideal sine wave form shall be symmetric in positive and negative polarities.



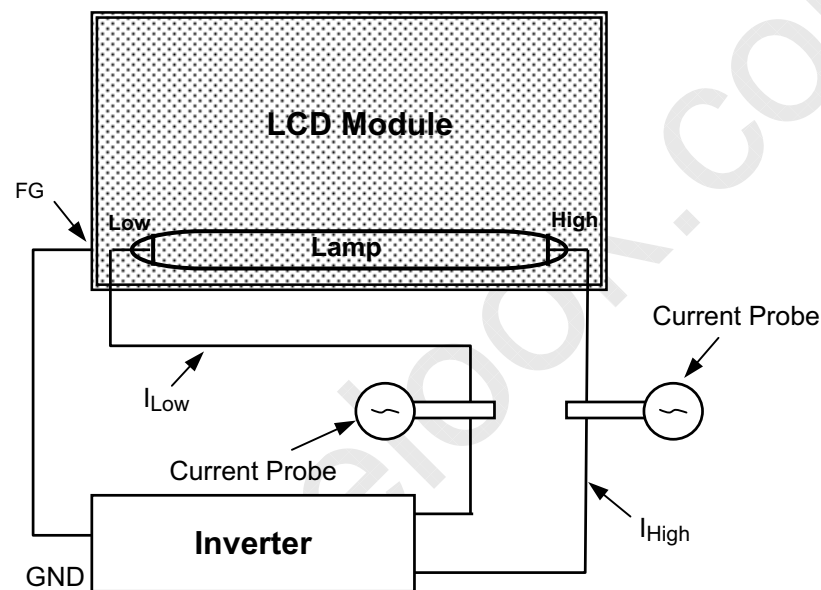
* Asymmetry rate:

$$|I_p - I_{-p}| / I_{rms} * 100\%$$

* Distortion rate

$$I_p \text{ (or } I_{-p}) / I_{rms}$$

Note (7) The lamp leakage current is measured by the current difference between in and out. And the measurement condition is as below:



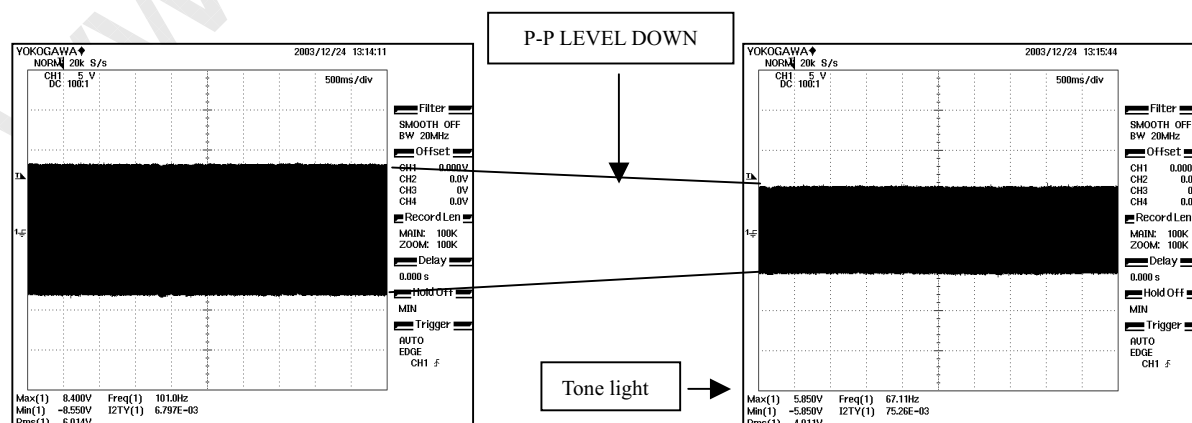
$$I_{Leak(RMS)} = I_{High(RMS)} - I_{Low(RMS)}$$

Note (8) About operating current min 2.0mA , lamp maker has some advice as below :

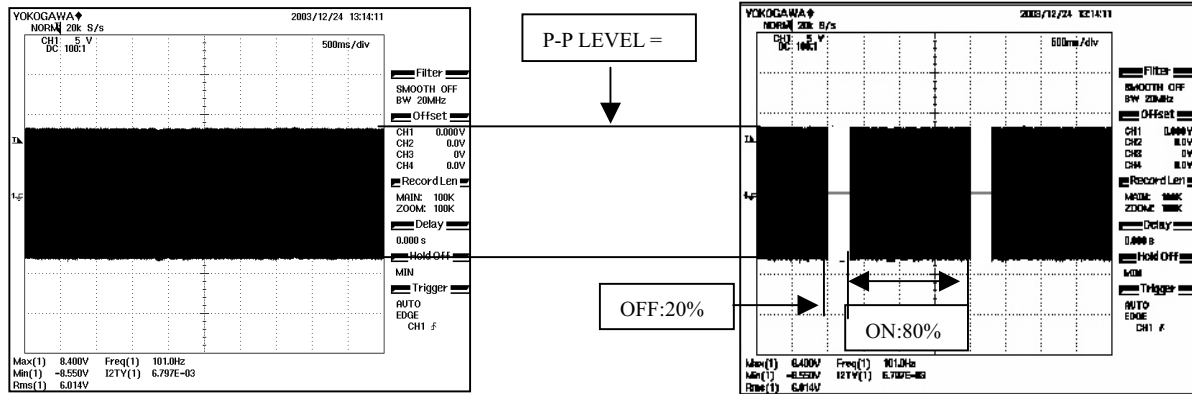
(Reference) Light quantity adjustment method

Explanation and comparison of the kind of tone light:

① Lamp current wave-like by the adjustment of the current.



- ② Lamp current wave-like by the adjustment of the burst.



Comparative table

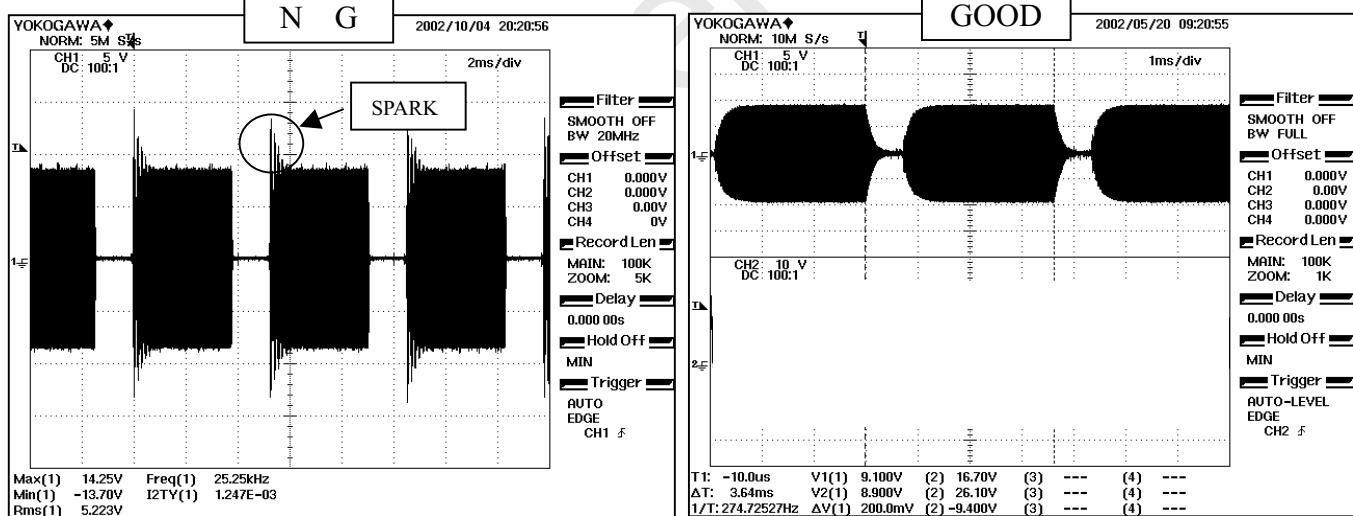
Method	Backlight efficiency (INV + LAMP)	Tone light rate (%)	Circuitry
①current	Good (75 % ~ 85%)	58	Complicated
②burst	Bad (65 % ~ 75%)	10	Easy

Method of case that Lamp current MIN2.0mA is controlled.

It is the setting of minimum 2.0mA (MIN) to Lamp current 6.0mA in the lamp specification. The burst is excellent for circuitry. The marker proposes that pays attention to the following contents.

The attention point of the light with a touch of the burst:

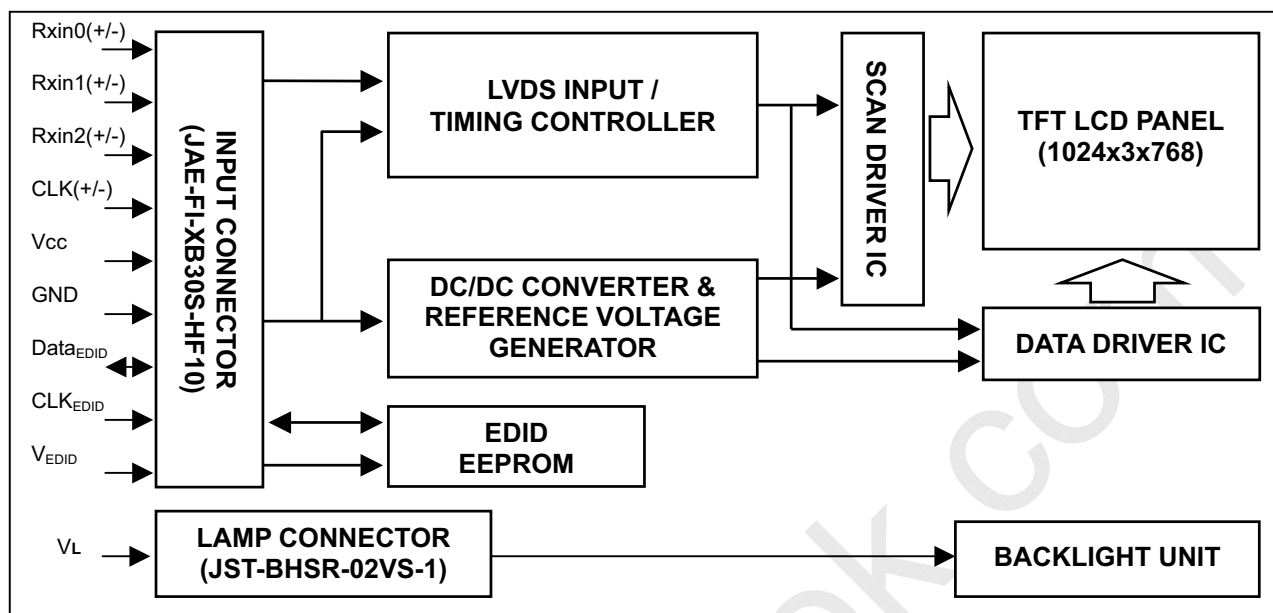
- ① Do not to be SPARK at start.



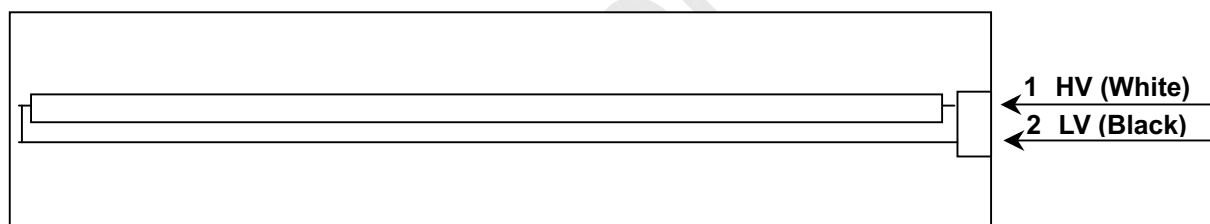
- ② PWM frequency does so that the frequency that is not able to divide the fixed number time, fixed number to lamp drive frequency is selected. (It is due to resonance noise occurrence prevention.) Even the frequency that is using it for LCD avoids selecting it.

4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



4.2 BACKLIGHT UNIT



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	Vcc	Power Supply +3.3 V (typical)		
3	Vcc	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		DDC 3.3V Power
5	NC	Non-Connection		
6	CLK _{EDID}	DDC Clock		DDC Clock
7	DATA _{EDID}	DDC Data		DDC Data
8	Rxin0-	LVDS Differential Data Input	Negative	R0~R5,G0
9	Rxin0+	LVDS Differential Data Input	Positive	
10	Vss	Ground		
11	Rxin1-	LVDS Differential Data Input	Negative	G1~G5,B0,B1
12	Rxin1+	LVDS Differential Data Input	Positive	
13	Vss	Ground		
14	Rxin2-	LVDS Differential Data Input	Negative	B2~B5,DE,Hsync,Vsync
15	Rxin2+	LVDS Differential Data Input	Positive	
16	Vss	Ground		
17	CLK-	LVDS Clock Data Input	Negative	LVDS Level Clock
18	CLK+	LVDS Clock Data Input	Positive	
19	Vss	Ground		
20	NC	Non-Connection		
21	NC	Non-Connection		
22	Vss	Ground		
23	NC	Non-Connection		
24	NC	Non-Connection		
25	Vss	Ground		
26	NC	Non-Connection		
27	NC	Non-Connection		
28	Vss	Ground		
29	NC	Non-Connection		
30	NC	Non-Connection		

Note (1) The first pixel is even.

Note (2) Connector Part No.: JAE- FI-XB30SRL-HF11 or equivalent

Note (3) User's connector Part No: JAE-FI-X30M or equivalent

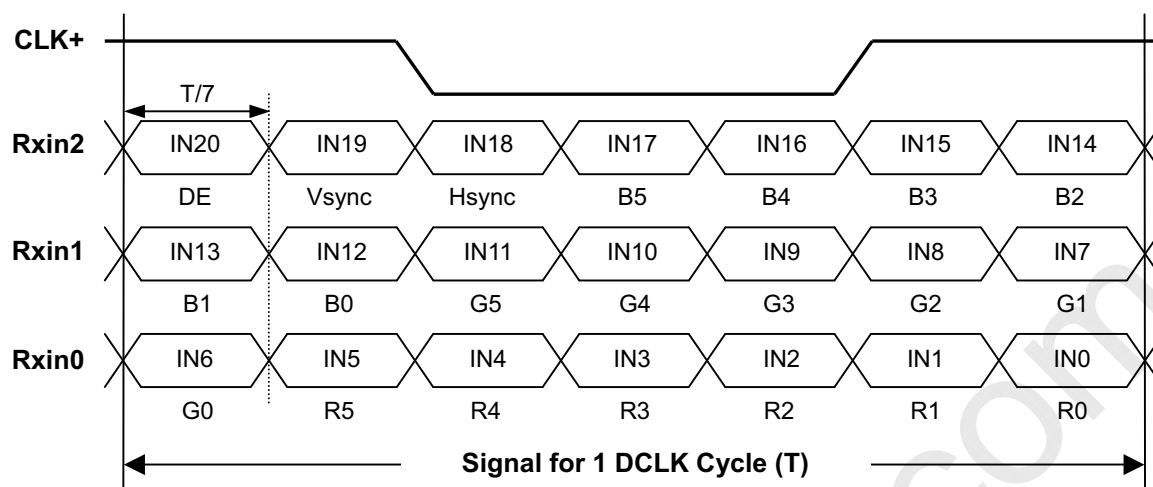
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	White
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header , Fixed	00	00000000
1	1	Header , Fixed	FF	11111111
2	2	Header , Fixed	FF	11111111
3	3	Header , Fixed	FF	11111111
4	4	Header , Fixed	FF	11111111
5	5	Header , Fixed	FF	11111111
6	6	Header , Fixed	FF	11111111
7	7	Header , Fixed	00	00000000
8	8	ID=IBM	24	00100100
9	9	ID=IBM	4D	01001101
10	0A	XGA (IBM Unique ID)	55	01010101
11	0B	XGA (IBM Unique ID)	0A	00001010
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture 1 - 53 (unused: 00h) : 02h fixed by CMO	00	00000000
17	11	Year of manufacture year - 1990(unsed:00h) : 0Dh (Year 2003) fixed by CMO	00	00000000
18	12	Version=1	01	00000001
19	13	Revision=3	03	00000011
20	14	Digital	80	10000000
21	15	Active area horizontal 28cm	1C	00011100
22	16	Active area vertical 21cm	15	00010101
23	17	gamma * 100-100 = 2.2*100-100=120	78	01111000
24	18	Feature support (no DPMS, Active off, RGB, Preferred Timing Mode)	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	B3	10110011
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	40	01000000
27	1B	Rx=0.57	91	10010001
28	1C	Ry=0.335	55	01010101
29	1D	Gx=0.325	53	01010011
30	1E	Gy=0.57	91	10010001
31	1F	Bx=0.15	26	00100110
32	20	By=0.125	20	00100000
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1024x768@60Hz)	08	00001000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001



40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("65MHz", According to VESA CVT Rev1.1)	64	01100100
55	37	65MHz/10000 =6500=1964H	19	00011001
56	38	HActive(D7-D0) = 1024 mod 256	00	00000000
57	39	HBlank(D7-D0) = 320 mod 256	40	01000000
58	3A	HActive(D11-D8) : HBlank(D11-D8) = 1024/256 : 320/256	41	01000001
59	3B	VActive(D7-D0) = 768 mod 256	00	00000000
60	3C	VBlank(D7-D0) = 38 mod 256	26	00100110
61	3D	VActive(D11-D8) : VBlank(D11-D8) = 768/256 : 38/256	30	00110000
62	3E	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 24	18	00011000
63	3F	HSyncWidth(D7-D0) = 136	88	10001000
64	40	VSynOffset(D3-D0)=3 : VSynWidth(D3-D0)=6	36	00110110
65	41	HSyncOffset(D9-D8) : HSyncWidth(D9-D8) : VSynOffset(D5-D4) : VSynWidth(D5-D4)	00	00000000
66	42	HImageSize(mm, D7-D0) = 285mod 256	1D	00011101
67	43	VImageSize(mm, D7-D0) = 214mod 256	D6	11010110
68	44	HImageSize(D11-D8) : VImageSize(D11-D8) = 285/256 : 214/256	10	00010000
69	45	Hborder=0	00	00000000
70	46	Vborder=0	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	18	00011000
72	48	Flag	00	00000000
73	49	Flag	00	00000000
74	4A	Flag	00	00000000
75	4B	Data type tag :0F	0F	00001111
76	4C	Flag	00	00000000
77	4D	Low Refresh Rate #1 (Horizontal active pixels / 8) - 31=97(61h)	61	01100001
78	4E	Low Refresh Rate #1 Image Aspect ratio(4 : 3)	43	01000011
79	4F	Low Refresh Rate #1 Refresh Rate=50Hz	32	00110010
80	50	Low Refresh Rate #2 (Horizontal active pixels / 8) - 31=97(61h)	61	01100001
81	51	Low Refresh Rate #2 Image Aspect ratio(4 : 3)	43	01000011
82	52	Low Refresh Rate #2 Refresh Rate=40Hz	28	00101000


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83	53	Brightness (1/10nit) , 150/10=15(=0Fh)	0F	00001111
84	54	Feature Flags	01	00000001
85	55	Reserved	00	00000000
86	56	EISA manufacturer code(3 Character ID) -CMO	0D	00001101
87	57	Compressed ASCII	AF	10101111
88	58	Panel Supplier Reserved - Product code -1407	07	00000111
89	59	(Hex, LSB first)	14	00010100
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data type tag :FEh	FE	11111110
94	5E	Flag	00	00000000
95	5F	"C"	43	01000011
96	60	"M"	4D	01001101
97	61	"O"	4F	01001111
98	62	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
99	63	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
100	64	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
101	65	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
102	66	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
103	67	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
104	68	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
105	69	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
106	6A	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
107	6B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data type tag : FEh	FE	11111110
112	70	Flag	00	00000000
113	71	"N"	4E	01001110
114	72	"1"	31	00110001
115	73	"4"	34	00110100
116	74	"1"	31	00110001
117	75	"X"	58	01011000
118	76	"C"	43	01000011
119	77	"_"	96	10010110
120	78	"L"	4C	01001100
121	79	"0"	30	00110000
122	7A	"1"	31	00110001

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OPTOELECTRONICS CORP.

Issued Date: May. 27, 2005

Model No.: N141XC -L01

Tentative

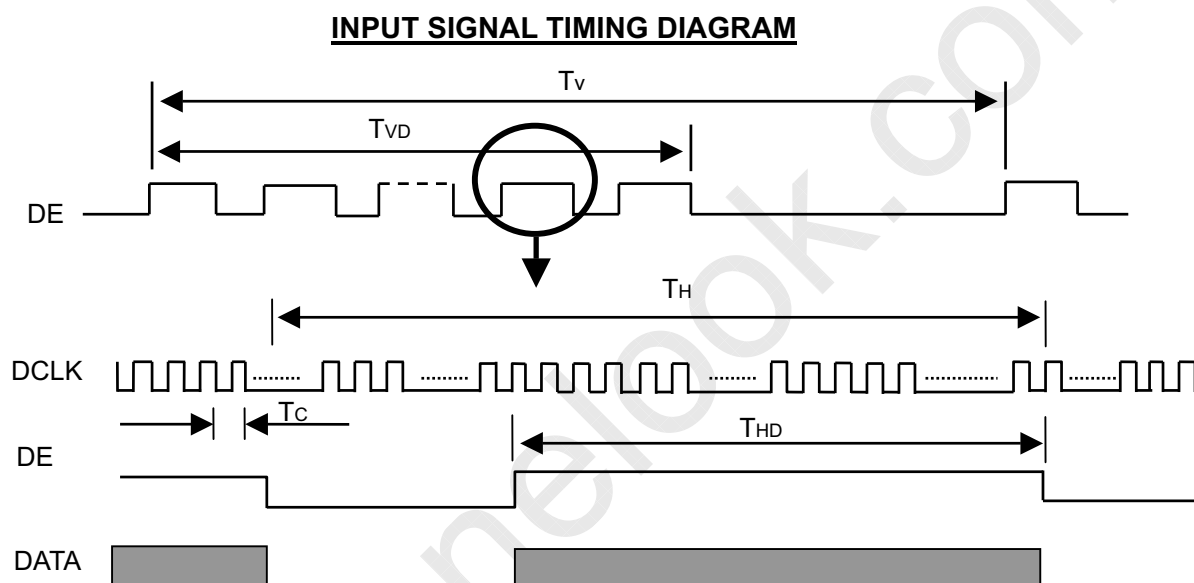
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	No extension	00	00000000
127	7F	One-byte checksum of entire 128 bytes EDID equals 00h.	52	01010010

6. INTERFACE TIMING

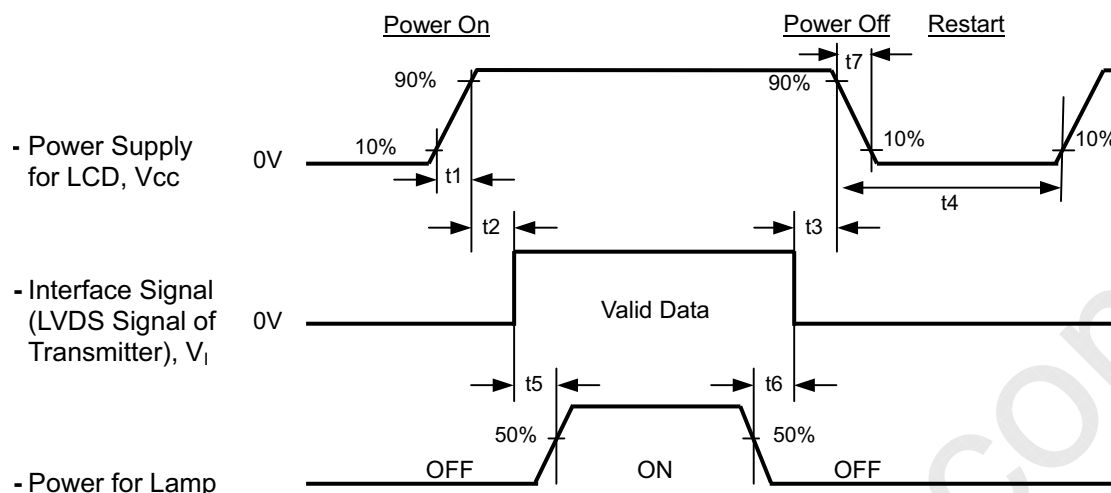
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	-	65	68	MHz	-
DE	Vertical Total Time	TV	770	806	818	TH	-
	Vertical Addressing Time	TVD	768	768	768	TH	-
	Horizontal Total Time	TH	1094	1344	1364	Tc	-
	Horizontal Addressing Time	THD	1024	1024	1024	Tc	-



6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$0.5 \leq t1 \leq 10 \text{ msec}$$

$$0 < t2 \leq 50 \text{ msec}$$

$$0 < t3 \leq 50 \text{ msec}$$

$$t4 \geq 500 \text{ msec}$$

$$t5 \geq 200 \text{ msec}$$

$$t6 \geq 200 \text{ msec}$$

Note (1) Please avoid floating state of interface signal at invalid period.

Note (2) When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time had better to follow

$$t7 \geq 5 \text{ msec}$$

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

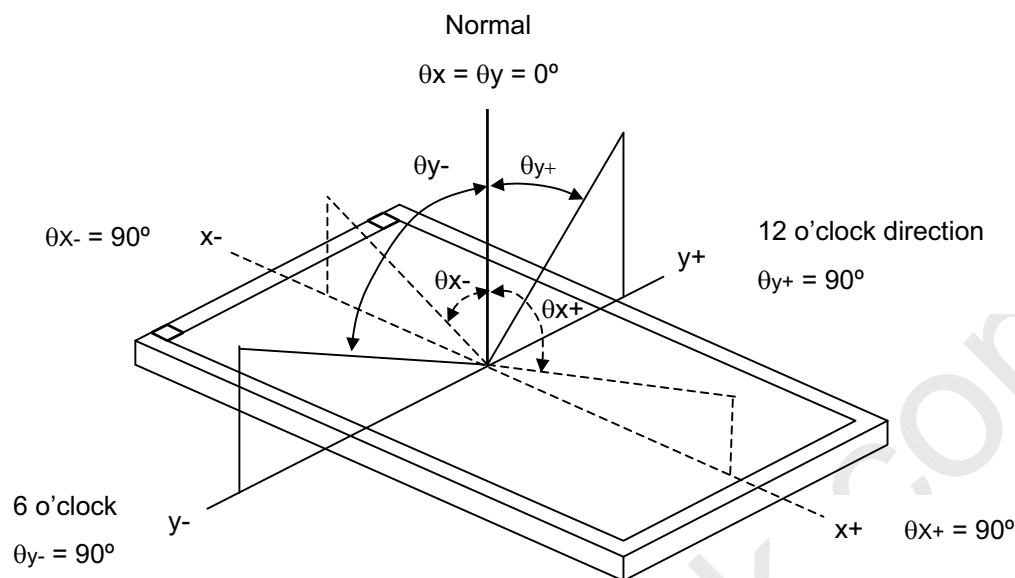
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Inverter Current	I _L	6.0	mA
Inverter Driving Frequency	F _L	60	KHz
Inverter	Sumida-H05-4915		

The measurement methods of optical characteristics are shown in Section 7.2. The following items should be measured under the test conditions described in Section 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	(180)	(300)	-	-	(2), (5)
Response Time		T _R		-	(5)	(10)	ms	(3)
		T _F		-	(11)	(16)	ms	
Luminance of White		L _{AVE}		(120)	(150)	-	cd/m ²	(4), (5)
White Variation		δW 5pts		-	-	(1.25)	-	(5), (6)
Color Chromaticity	Red	R _x		TYP -0.03	TBD	TYP +0.03	-	(1)
		R _y			TBD		-	
	Green	G _x			TBD		-	
		G _y			TBD		-	
	Blue	B _x			TBD		-	
		B _y			TBD		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
Viewing Angle	Horizontal	θ_{x+}	CR≥10	(40)	(45)	-	Deg.	
		θ_{x-}		(40)	(45)	-		
	Vertical	θ_{y+}		(15)	(20)	-		
		θ_{y-}		(40)	(45)	-		

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

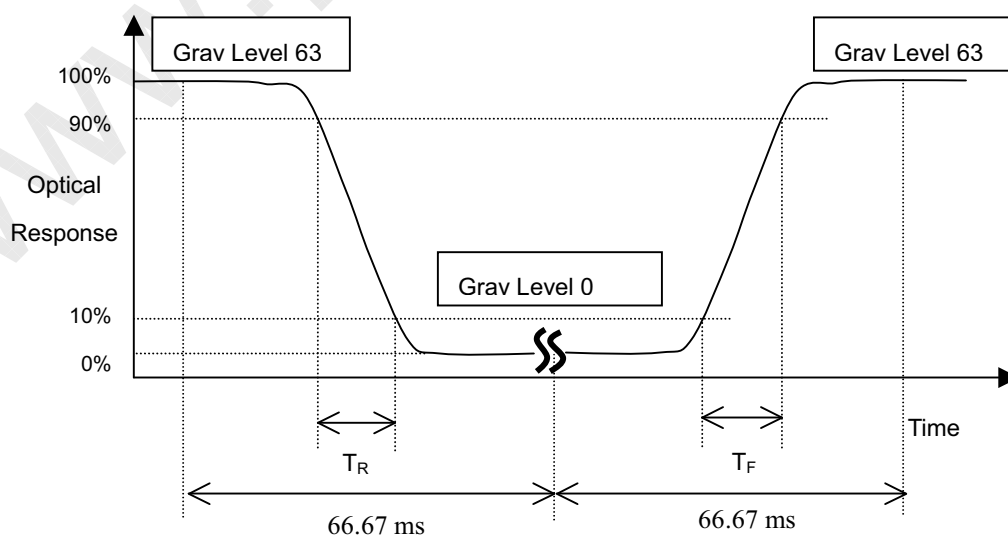
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (7).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

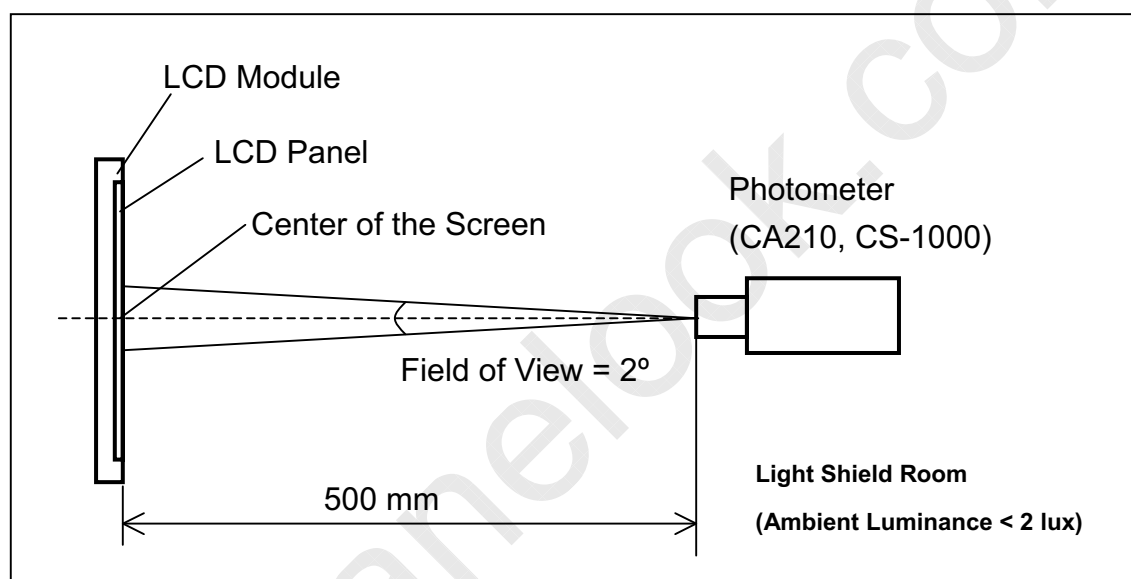
Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(1) + L(2) + L(3) + L(4) + L(5)] / 5$$

$L(x)$ is corresponding to the luminance of the point X at Figure in Note (7).

Note (5) Measurement Setup:

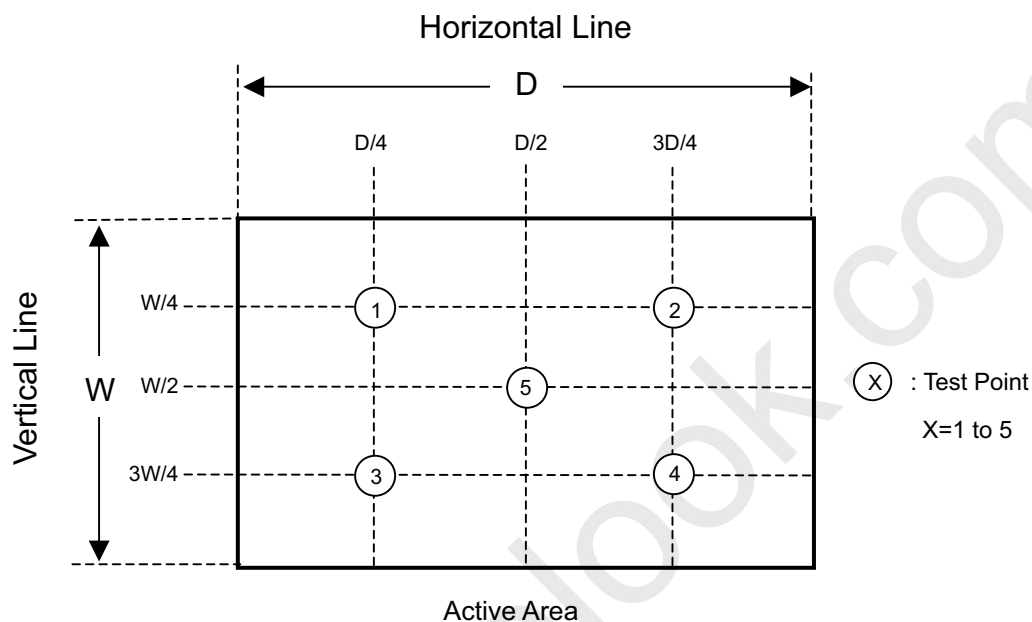
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 63 at 5 points

$$\delta W_{5p} = \text{Maximum } [L(1) \sim L(5)] / \text{Minimum } [L(1) \sim L(5)]$$



8. PRECAUTIONS

8.1 HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

8.2 STORAGE PRECAUTIONS

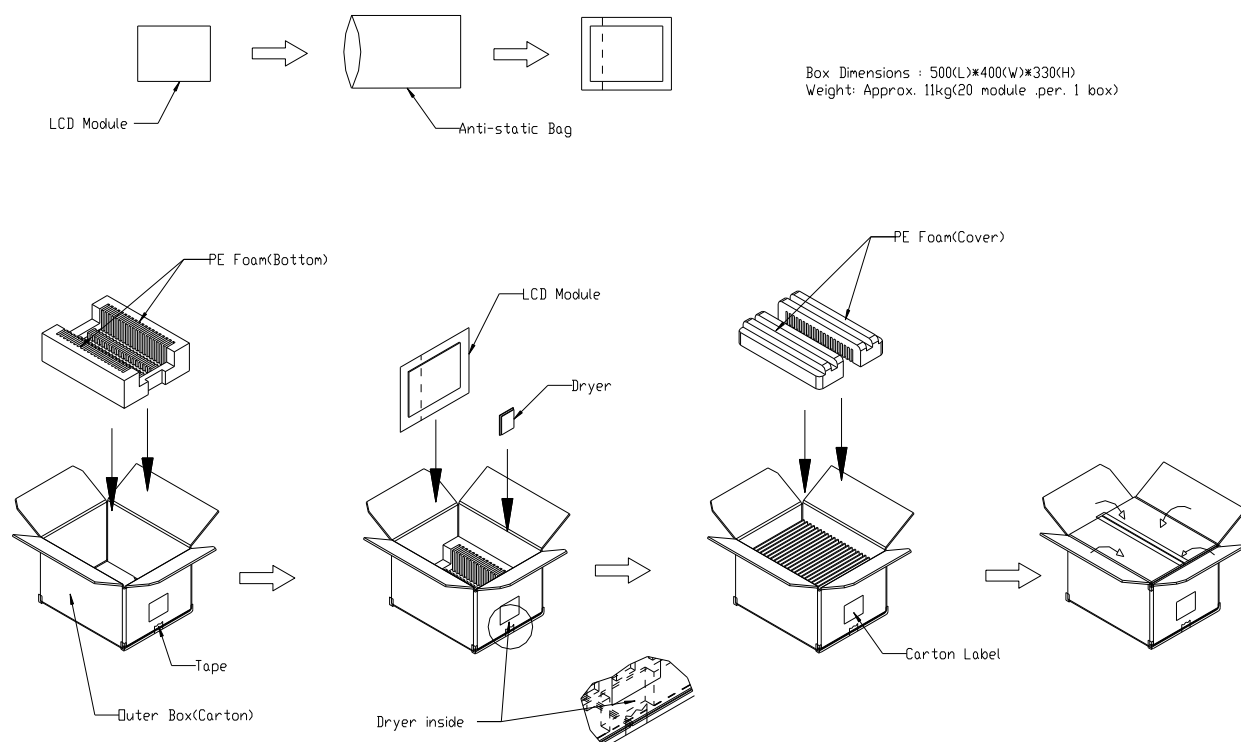
- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

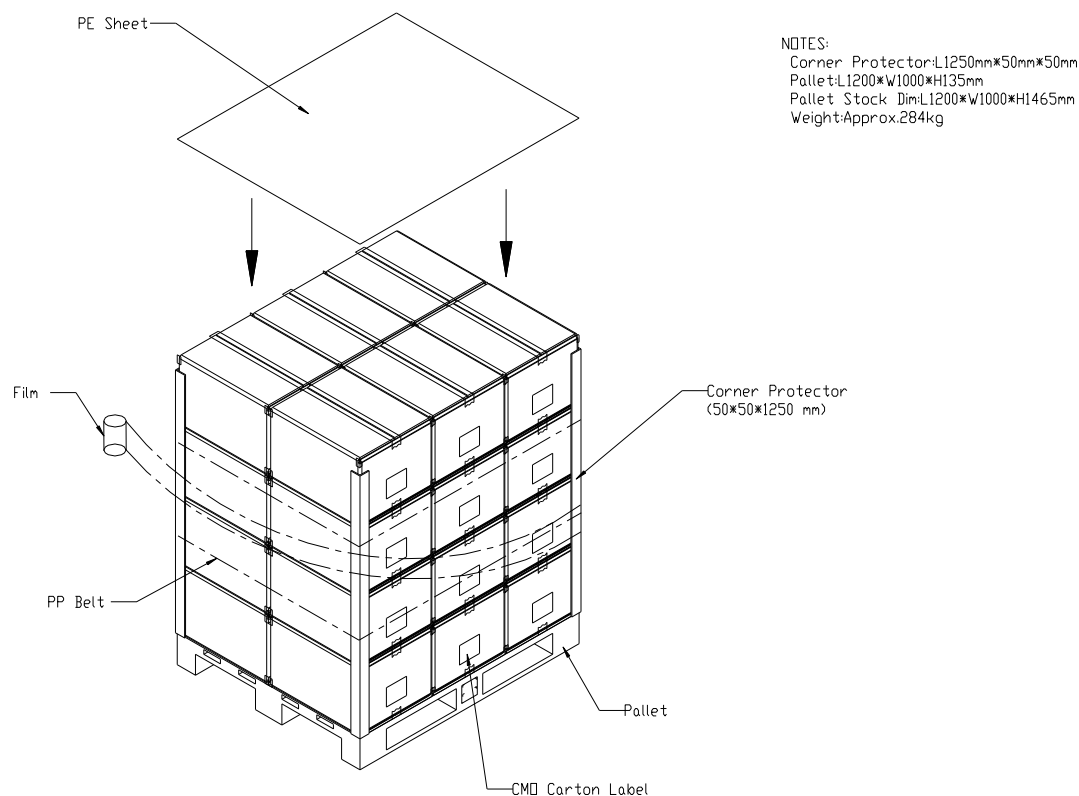
- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9. PACKING

9.1 CARTON



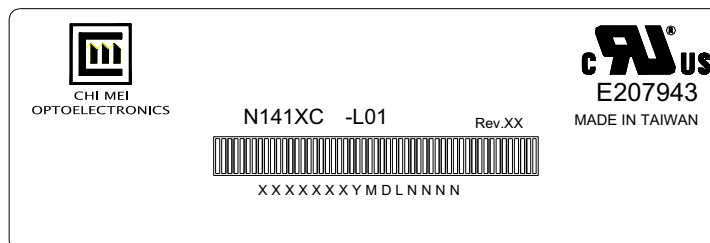
9.2 PALLET



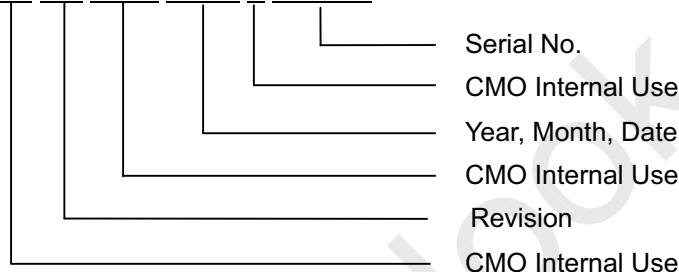
10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



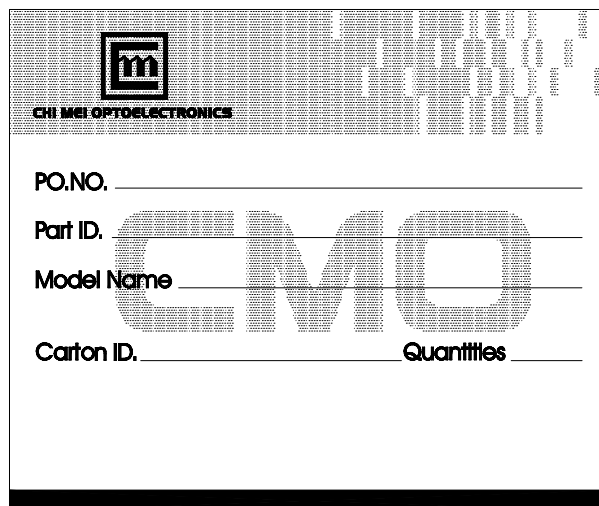
- (a) Model Name: N141XC - L01
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: XXXXXXXXYMDXXNNNN

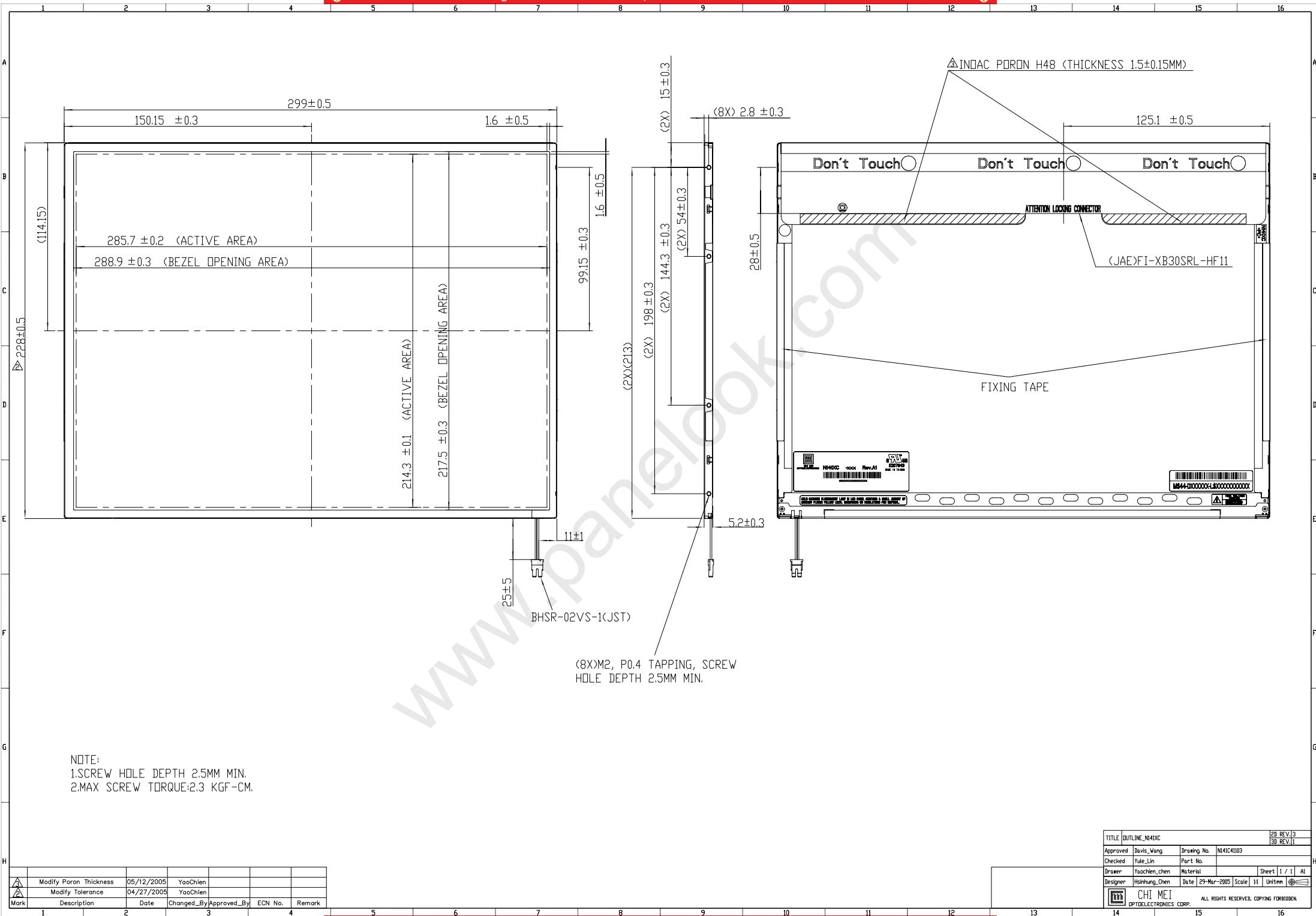


Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

10.2 CARTON LABEL





Modify Poron Thickness	05/12/2005	YaoChien			
Modify Tolerance	04/27/2005	YaoChien			
Description	Date	Changed_By	Approved_By	ECN No.	Remark

TITLE OUTLINE_N41XC		2D REV.3	
Approved Davis_Wang		3D REV.1	
Checked Yule_Lin	Drawing No. N41C4103		
Drawer YaoChien_chen	Part No.		
Designer HsinHung_Chen	Material		
Date 29-Mar-2005	Scale 1:1	Sheet 1 / 1	Alt
CHI MEI OPTOELECTRONICS CORP.		ALL RIGHTS RESERVED. COPYING FORBIDDEN	